Integrated Wireless MEMS Accelerometer for Physiological Activity Monitoring

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ABSTRACT

A wireless MEMS accelerometer for physiological activity monitoring, which is light weight and consumes low power, is proposed. The device is intended to acquire the movement and vibration signal from human body. It processes and transmits the signal wireless to a nearby base station using 900 MHz ISM band.

Keywords: MEMS, Accelerometer, Interface Circuit, Capacitive sensing, Wireless transmitter.

1. INTRODUCTION

In the last 50 years the world is blessed by thousands of electronic products since the first transistor is invented in 1947. Electrical engineers relentlessly pushed the limits all around the field to improve the quality of human life. While numerous medical and technological innovations increased the life expectancy by 15 to 20 years, they also provided disadvantaged people the ray of new light towards a normal life. Hearing aids provided the hearing impaired to hear, laser surgery provided the sight impaired to see, diagnostic equipment detected fatal diseases early to cure and the list goes on. The motivation for this work is to contribute to better the human life further.

Accurate data on physical movements and vibrations of muscles may help a physician to determine a physiological condition of a patient. It may help physical therapist to find a way to eliminate or improve someone’s disability. Coaches may be able to know how the athletes are performing and improving. Exercise and fitness equipment manufacturers may want to know how their products are affecting human bodies. To provide the answer to these issues, a product is proposed here that can sense the movement and vibration of the human body. The proposed device is a tiny little sensor with six degrees of freedom that can operate from a coin cell battery for several hours and can be placed on human skin using tapes. The device also transmits the acquired signal wireless to a nearby base station, which could be a laptop with an RF receiver. Multiple of these devices can form a network to provide a larger picture on physiological movements.

To keep the initial implementation simple we are considering a lateral axis acceleration signal only at this stage. Therefore, the proposed device is a MEMS (Microelectromechanical Systems) accelerometer with CMOS readout, conditioning and transmitting circuits integrated on a single chip. To the best of our knowledge single-chip wireless accelerometers haven’t been demonstrated using traditional CMOS process. Several surface micromachining accelerometers with continuous time readout circuits using chopper stabilization technique are reported [1-3]. Microstrain developed a wireless accelerometer [4] that uses analog devices' ADXL2XXJE accelerometer with few other chips on a board. A wireless accelerometer is reported in [5] where MEMS and Surface acoustic devices are integrated. It does not require any on board power supply at sensor location. In [6], a multi-functional input devices system (MIDS) is reported where Analog Devices' accelerometers sense the multi axis motion in the finger rings, and a MIDS wrist watch communicates with the rings and transmits data wirelessly to interface with a PC.

A generic block diagram of the proposed wireless accelerometer is given in Fig. 1. It has four main building blocks: MEMS transducer, readout circuit, analog to digital (A/D) converter and an RF transmitter. One bit quantized sigma delta A/D converter output may be used for force feedback control of the transducer.

![Block diagram of the wireless accelerometer](image)

Fig. 1: Block diagram of the wireless accelerometer

2. MEMS ACCELEROMETER

A CMOS MEMS accelerometer can be modeled as a proof mass, spring and damping system all realized by
When the accelerometer chip experiences an external acceleration, the proof mass moves due to the inertial force. The displacement of the proof mass in turn causes a spring elastic force. A viscous damping force will also act on the proof mass. As a result the differential equation in the sensing axis that governs the force-displacement relation is given by

\[ F_{in}(t) = ma_{in}(t) = m \frac{d^2 x(t)}{dt^2} + b \frac{dx(t)}{dt} + kx(t). \]  

(1)

\[ \Rightarrow \frac{d^2 x(t)}{dt^2} + \frac{\omega_n}{Q} \frac{dx(t)}{dt} + \omega_n^2 x(t) = a_{in}(t), \]  

(2)

where, \( \omega_n \) = resonance frequency of the system = \( \sqrt{\frac{k}{m}} \), \( b \) is damping coefficient, and \( Q \) = mechanical quality factor = \( \frac{\sqrt{km}}{b} \). Now in \( s \) domain the transfer function is derived as

\[ T(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2}. \]  

(3)

Human motion is limited to few tens of Hz. The resonance frequency of the microsensor is about a few kHz. As a result, at frequencies much smaller than resonance frequency,

\[ T(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{\omega_n^2}. \]  

Consequently, mechanical sensitivity of the accelerometer is:

\[ \frac{x}{a_{in}} = \frac{1}{\omega_n^2} = \frac{m}{k}. \]  

(4)

**Capacitance Sensing**

The CMOS MEMS accelerometer is designed such that it has two sets of capacitive comb fingers. Rotor fingers are mechanically attached to the proof mass and hence are movable. On the other hand, stator fingers are rigidly attached to the substrate and thus are stationary. While an external acceleration causes the proof mass to move along with the rotor fingers, as shown in Fig. 3, the gaps between the rotor and the stator fingers change, creating a change in the inter finger capacitances. The capacitance \( C_1 \) increases and \( C_2 \) decreases as the gap decreases, and these changes are proportional to the acceleration. The principal design objective of the CMOS accelerometer is to convert this mechanical displacements hence the capacitive change into the electrical signal efficiently. To perform this objective an electrical signal \( V_m \) is applied in the stator fingers that creates a sensing signal \( V_s \).

The accelerometer has a fully differential bridge for capacitive sensing as shown in Fig. 4, where \( C_p \) represents the total parasitic capacitance at the sensing node. A sensor is usually designed fully differential that provides the fully differential signals to the following readout circuit with a very good common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). This also eliminates the need for common mode feedback (CMFB) circuits at the front end.

\[ V_s = \frac{4C_1}{2C_1 + C_p} \frac{x}{x_0} V_m. \]  

(5)

Using (4) we get the sensitivity of the accelerometer as

\[ a_{in} = \frac{4C_1}{2C_1 + C_p} \frac{V_m}{x_0} \frac{1}{\omega_n^2}. \]  

(6)

### 3. INTERFACE CIRCUIT

An electronic system with a dynamic range (DR) as high as 100 dB that operates more than 20 hours from a single coin cell battery is proposed. Direct amplification of DC
or very low frequency signal which is as low as few tens of nV at the sensing nodes is corrupted by the large 1/f (flicker) noise and the circuit DC offset. Therefore, to avoid such problems the chopper stabilization technique [7] (Fig. 5) is used where modulation signals are applied to the sensor to transpose the signal to a 5 MHz frequency, where there is no or significantly lower flicker noise. Then the signal is amplified and demodulated back to the base band. Simulation shows that the higher modulation frequency reduces the overall noise floor, but increases the power consumption.

![Fig. 5: Chopper stabilized circuit architecture](image)

A chopper stabilized readout circuit is designed and fabricated using TSMC 0.35 µm CMOS technology. The fabricated chip is currently in the phase of releasing MEMS structures using bulk CMOS post processing [8]. The power consumption of the CMOS interface circuits is 5 mW from a 3 V supply.

The extracted view of the layout of the readout circuit is given in Fig 6. The top metal of the 4 metal, 2 poly CMOS process is used to cover the CMOS circuits to protect them during the etching in the post CMOS processing.

![Fig. 6: Extracted view of the readout circuit layout](image)

The preamplifier is designed in two stages. The first stage is optimized for optimum input noise floor and a wideband operational transconductance amplifier second stage for gain. Since the proposed chip houses both the digital and the analog circuits, a fully differential architecture is highly desirable. The differential architecture provides better CMRR and PSRR amidst noisy substrate, power supplies and overall environment. During simulation, the preamplifier provides an overall gain of about 50 dB and a 3-dB bandwidth of 8 MHz (Fig. 7) with an output swing of about 1.6 V from a 3 V supply. The input referred electronic noise floor is 40 nV (Fig. 8). In the amplifier, two auxiliary input pairs are included for DC and sensor offset cancellation [2, 7].

A demodulator follows the preamplifier circuits (Fig. 9). Clock signals generate the modulation signals, the input bias reset signal and the demodulator clocks are generated using digital circuits. The transient simulation results of the readout circuit are given in Fig. 10. FFT of the preamplifier output shows the fundamental component of the waveform which is 5 MHz. The FFT of the demodulator output is at d.c., which is expected after demodulation. Conversion gain for the demodulator is about 0.6.

![Fig. 7: Frequency response of the preamplifier](image)

The output common mode level is set by a CMFB network. An on-chip capacitance along with a resistor compensates for the potential instability in the CMFB loop. Cascode current mirrors are used to boost the output resistances of the tail current sources which improve the CMRR and the PSRR of the differential amplifier. An input biasing circuit is included in the preamplifier to set the input DC bias voltages. This topology is robust against the charging and the leakage activity at the input nodes.
Noise
There are two kinds of noises in CMOS MEMS accelerometer: the thermal-mechanical Brownian noise from the mechanical sensor and the electronic noise from the readout circuit. Fig. 11 shows the sources of electronic noises in the readout circuit.

Increasing the current through the input transistor reduces the noise floor. However, this improvement is costly, since a 2x reduction in noise requires a 16x increase in the drain current, and therefore, the power consumption increases. The capacitive matching technique is applied to optimize the input stage for the minimum noise floor.

Sensor Offset Cancellation
The manufacturing mismatches create unbalance in the sensing capacitances in the capacitance bridge. As a result, even when the accelerometer is in its rest position, this capacitance offset appears as a constant (DC) signal at the sensing nodes. Modulated by the high frequency modulation signal, this signal can not be eliminated by a ac coupling or filtering and can only be removed by either trimming or calibration. The sensor offset cancellation can be done in mechanical domain by using electrostatic actuators to pull the proof-mass back to the center position. However, for large sensor offset, large actuator area and high voltage are needed. It is therefore very desirable to have an electronic cancellation of the sensor offset.

An auxiliary arm to the second stage of the amplifier is used to provide a correction signal necessary to cancel the sensor offset which appears as a 5 MHz carrier. Fig. 12 shows a proposed circuit, where a 5 MHz signal is applied to a resistive divider. One of the resistors, R2, is off chip and will be tuned to generate the exact voltage necessary to cancel the offset. The polarity of the voltage applied to the resistive divider can be set by a switch network depending on the polarity of the sensor offset.

A signal of 5 MHz, 1mV sine wave with an amplitude modulation (AM) frequency of 1 MHz and a modulation index of 1 is applied at the input of the preamplifier for simulation purpose to mimic the presence of a sensor offset (at 5MHz). Fig. 13 shows that an attenuation of 26 dB is achieved in simulation with a correction signal applied.
Circuit DC Offset Cancellation
A low pass filter (LPF) in the feedback path appears as a high pass filter (HPF) in the signal path. This filter attenuates the circuit DC offset and the low frequency noise. The LPF is realized using a simple differential amplifier with an off-chip capacitance. A capacitance of 500pF provides a high pass filtering with a -3-dB frequency at around 500 KHz as it appears in Fig. 7. A higher capacitance provides a lower -3-dB frequency.

An intentional DC offset is created through a transistor mismatch for simulation. Fig. 14 shows that with no DC offset cancellation circuit DC offset is 793 mV and with a DC offset cancellation circuit it is 1 mV. Thus, a 58 dB attenuation to DC offset is achieved.

Sigma Delta A/D Converter
The proposed accelerometer has a range of ±2 g and a resolution of 20 µg. Therefore, the input dynamic range of this system is 100 dB. If the bandwidth \( f_B \) of the signal is 1 KHz, a second order sigma delta (ΣΔ) analog to digital converter [9] with 1-bit quantizer and oversampling ratio of 256 provides a dynamic range of 109 dB (17 bits resolution).

4. WIRELESS ARCHITECTURE
The overall architecture of the system is given in Fig. 9. To keep the complexity of the wireless accelerometer minimum, only a transmitter is considered. Although an AM scheme that keeps signal path analog all along is the simplest and least power hungry choice among all options, however the output stages can not provide a 100 dB DR without introducing a significant nonlinearity.

In the proposed architecture, the digitized signal is applied to a passive mixer [10] through buffers. The mixer modulates the digital signal and up-converts to 910 MHz. Since the input of the mixer has two states, on or off, the modulation scheme is essentially amplitude shift keying (ASK) or on-off-Keying. The mixing signals at the gate of the switching transistors are generated by an LC oscillator that uses off chip inductor and capacitor. The up-converted signal centered at 910 MHz is then applied to a power amplifier (PA) to provide the necessary power to a 50 Ω off-chip antenna through an output impedance matching. Since the transmitting signal is constant envelop, the PA can be either linear or non linear. A small antenna in the order of few millimeters is required to keep the overall implementation small.

Passive Mixer
To implement the up-conversion mixer in a CMOS technology the MOS switch based double balanced passive mixer (Fig. 9) is an excellent choice for number of reasons. Although the conversion gain of a passive mixer is always less than unity, it does not consume any power. Another advantage is the inherent linearity of the switching mixer due to the good linearity of the MOS devices operated in the linear region. In passive mixer the bias current through the transistors is zero leading to low flicker noise. This is a very important advantage considering direct up-conversion architecture of the proposed architecture. The main source of error in this mixer is the non-symmetry in the devices or in the driving voltages.

In this design, 100 µm transistor switches are used, the input bias is 1.3 V and the LO bias is 2 V. The oscillator is designed to provide an LO amplitude of 1 V. The simulated performances of the designed mixer are given in Fig. 15.

LC Oscillator
The complementary LC oscillator [11] (Fig. 9) is used in this design that has both NMOS and PMOS transistors to maximize the use of the bias current though the oscillator. It also allows to set the DC bias of the output LO signal which is very critical for efficient operation of the switching mixer. The use of an off-chip inductor saves power. It also avoids a phase lock loop to tune the frequency while keeping the implementation simple. The simulated oscillator phase noise is given in Fig. 16.

5. SUMMARY
An integrated wireless MEMS accelerometer (specifications in Table 1) is proposed that uses the chopper stabilization technique in the readout circuit and ASK modulation for transmission. The system is
designed for high dynamic range and low power. It also cancels the DC and sensor offsets.

Table 1: Overall specifications of the accelerometer

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value/Comments</th>
</tr>
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<tbody>
<tr>
<td>Power consumption</td>
<td>15 mW</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>100 dB</td>
</tr>
<tr>
<td>Freq. of transmission</td>
<td>900 MHz ISM band</td>
</tr>
<tr>
<td>Power supply</td>
<td>Single 3 V coin-cell battery</td>
</tr>
<tr>
<td>Transmitting antenna</td>
<td>50 Ω external antenna</td>
</tr>
<tr>
<td>Wireless distance</td>
<td>10 meter with a micro-antenna or 200 meter with a quarter wave antenna.</td>
</tr>
<tr>
<td></td>
<td>Fully integrated with few off-chip passive components.</td>
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</tbody>
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Fig. 15: (a) Gain, (b) 1 dB compression point, and (c) noise figure of the mixer

Fig. 16: Phase noise of the oscillator.

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REFERENCES